Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Please cancel claims 42-45 without prejudice.

Claims 1-2 (cancelled)

3. (previously presented): An apparatus for the two cycle computation of a plurality of types of complex multiplication, the apparatus comprising:

a first storage means for storing a first complex operand and a second complex operand, the first complex operand including real component Xr and imaginary component Xi, the second complex operand including real component Yr and imaginary component Yi;

multiplier means for simultaneously performing multiplications in a first cycle of operation to produce products Xr*Yr, Xr*Yi, Xi*Yr and Xi*Yi, the multiplier means comprising an input to receive a signal indicating a type of complex multiplication to be performed;

a second storage means for storing products Xr*Yr, Xr*Yi, Xi*Yr and Xi*Yi;

adder means for simultaneously performing additions and subtractions in a second cycle of operation to produce a conjugated or nonconjugated result depending on the type of complex multiplication to be performed, said multiplier means routing produced products to the second storage means in response to the received signal indicating the type of complex multiplication to be performed and aligning the produced products in the second storage means for subsequent addition or subtraction with each other, the adder means comprising an input to receive the signal

indicating the type of complex multiplication to be performed, the adder means adding or subtracting the aligned produced products in response to the received signal;

a third storage means for storing the results of said adder means;

accumulator means for simultaneously performing accumulation in the second cycle of operation to accumulate the results of said adder means with the current contents of said third storage means, wherein said third storage means is further for storing the results of said accumulator means; and

extended precision storage means for storing an interim result, wherein said accumulator means is further for simultaneously performing accumulation in the second cycle of operation to accumulate the results of said adder means with both the current contents of said third storage means and the interim result stored in said extended precision storage means,

wherein said extended precision storage means stores extended precision results of said accumulator means at the completion of the accumulation means.

4. (original): The apparatus of claim 3 wherein:

the complex operand components Xr, Xi, Yr and Yi are each 16 bits,

the real and imaginary results are each 32 bits, and

the extended precision results are each 8 bits.

5. (previously presented): The apparatus of claim [[1]]3 wherein:

the complex operand components Xr, Xi, Yr and Yi are each 16 bits, and

the real and imaginary results are each 32 bits.

6. (previously presented): The apparatus of claim [[1]]3 wherein the multiplier means is further for simultaneously performing multiplications in the second cycle of operation utilizing a second pair of operands.

Claims 7-16 (canceled).

17. (previously presented): An apparatus for the single cycle computation for a plurality of types of complex multiplication, the apparatus comprising:

a first storage means for storing a first complex operand and a second complex operand, the first complex operand including real component Xr and imaginary component Xi, the second complex operand including real component Yr and imaginary component Yi;

multiplier means for simultaneously performing multiplications in a first cycle of operation to produce products Xr*Yr, Xr*Yi, Xi*Yr and Xi*Yi, the multiplier means comprising an input to receive a signal indicating a type of complex multiplication to be performed;

adder means for simultaneously performing additions and subtractions in the first cycle of operation to produce a conjugated or nonconjugated result depending on the type of complex multiplication to be performed, said multiplier means routing produced products to the second storage means in response to the received signal indicating the type of complex multiplication to be performed and aligning the produced products in the second storage means for subsequent addition or subtraction with each other, the adder means comprising an input to receive the signal

indicating the type of complex multiplication to be performed, the adder means adding or subtracting the aligned produced products in response to the received signal;

a third storage means for storing the results of said adder means; and

accumulator means for simultaneously performing accumulation in the first cycle of operation to accumulate the results of said adder means with the current contents of said third storage means, wherein said third storage means is further for storing the results of said accumulator means

extended precision storage means for storing an interim result, wherein said accumulator means is further for simultaneously performing accumulation in the first cycle of operation to accumulate the results of said adder means with both the current contents of said third storage means and the interim result stored in said extended precision storage means, wherein said extended precision storage means stores extended precision results of said accumulator means at the completion of the accumulation means.

18. (original): The apparatus of claim 17 wherein:

the complex operand components Xr, Xi, Yr and Yi are each 16 bits,

the real and imaginary results are each 32 bits, and

the extended precision results are each 8 bits.

19. (previously presented): The apparatus of claim [[15]]17 wherein:

the complex operand components Xr, Xi, Yr and Yi are each 16 bits, and

the real and imaginary results are each 32 bits.

20. (previously presented): The apparatus of claim [[15]]17 wherein the multiplier means is further for simultaneously performing multiplications in a second cycle of operation utilizing a second pair of operands.

21. (previously presented): The apparatus of claim [[15]]17 further comprising:

a logical array coupled to the multiplier means and the adder/accumulator means, said logical array aligning the produced products to determine which produced products are added to or subtracted from each other based on the type of complex multiplication being performed.

Claims 22-38 (cancelled).

39. (previously presented): An apparatus for the two cycle computation of a plurality of complex multiplication, the apparatus comprising:

a first storage register for storing a first complex operand and a second complex operand, the first complex operand including real component Xr and imaginary component Xi, the second complex operand including real component Yr and imaginary component Yi;

a multiplier for simultaneously performing multiplications in a first cycle of operation to produce products Xr*Yr, Xr*Yi, Xi*Yr and Xi*Yi, the multiplier means comprising an input to receive a signal indicating a type of complex multiplication to be performed;

a second storage register for storing products Xr*Yr, Xr*Yi, Xi*Yr and Xi*Yi;

an adder for simultaneously performing additions and subtractions in a second cycle of operation to produce a conjugated or nonconjugated result depending on the type of complex multiplication to be performed, said multiplier means routing produced products to the second storage means in response to the received signal indicating the type of complex multiplication to

be performed and aligning the produced products in the second storage means for subsequent addition or subtraction with each other, the adder comprising an input to receive the signal indicating the type of complex multiplication to be performed, the adder means adding or subtracting the aligned produced products in response to the received signal;

a third storage register for storing the results of said adder means;

an accumulator for simultaneously performing accumulation in the second cycle of operation to accumulate the results of said adder with the current contents of said third storage register, wherein said third storage register is further for storing the results of said accumulator; and

an extended precision storage register for storing an interim result, wherein said accumulator is further for simultaneously performing accumulation in the second cycle of operation to accumulate the results of said adder with both the current contents of said third storage register and the interim result stored in said extended precision storage means, wherein said extended precision storage register stores extended precision results of said accumulator at the completion of the accumulator.

40. (original): The apparatus of claim 39 wherein:

the complex operand components Xr, Xi, Yr and Yi are each 16 bits,

the real and imaginary results are each 32 bits, and

the extended precision results are each 8 bits.

41. (previously presented): The apparatus of claim [[37]]39 wherein:

the complex operand components Xr, Xi, Yr and Yi are each 16 bits, and

the real and imaginary results are each 32 bits.

claims 42-45 (canceled)